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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/854,095	05/11/2001	James E. Kocol	SUN-P5390-RJL	7707

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EXAMINER	
DOOLEY, MATTHEW C	
ART UNIT	**PAPER NUMBER**
2133	3

DATE MAILED: 03/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/854,095	KOCOL ET AL.	
	Examiner	Art Unit	
	Matthew C. Dooley	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 May 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 May 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chaudhry et al., U.S. 2002/0157056 in view of Arimilli et al., U.S. 6,480,975.

As per claim 1:

Chaudhry teaches to a memory system that includes a main memory controller, processor cache, a communication channel between the memory channel and the cache, and error detection and correction mechanisms within the memory controller (Fig.1B). The error detection and correction mechanism alters data and stores a corrected copy of the data in the main memory (Fig.2, 4). However, there is not an explicit teaching to the reading of a valid copy of the data checked out to the processor cache. Arimilli teaches to reading of a valid copy of the data checked out to the processor cache and the correction of the cached data (Col.2: 10-17; Col.4: 32-52). Therefore, it would have been obvious for one of ordinary skill in the art at the time of the invention to make use of the reading of a valid copy of the data checked out to the processor cache and the correction of the cached data of Arimilli, in conjunction with the changed and re-stored data system of Chaudhry because the addition of the circuitry of Arimilli allows for faster overall

operation of the circuitry by avoiding unnecessary ECC circuit operations (Arimilli: Col.4: 65-67).

As per claim 2:

Both Chaudhry [0013] and Arimilli (Col.4: 24-26) teach to single bit correction, double bit detection systems.

As per claim 3:

Arimilli (Col.4: 24-26) teaches to double bit correction systems (Col.4: 57-58).

As per claim 4:

Chaudhry teaches to I/O cache and to storage of an altered data copy in memory (Fig.2, 4). Moreover, the combination of Chaudhry with Arimilli disclosed above can further be applied here with respect to the reading of data from the cache when a copy of valid data is put into the cache, and correction of said data for re-storing in the memory.

As per claim 5:

Chaudhry teaches to a secondary processor cache and to storage of an altered data copy in memory (Fig.2, 4). Moreover, the combination of Chaudhry with Arimilli disclosed above can further be applied here with respect to the reading of data from the cache when a copy of valid data is put into the cache, and correction of said data for re-storing in the memory.

As per claim 6:

Chaudhry teaches to circuitry that recognizes the data in the cache pulled from the memory in the cache circuitry for the processor, I/O cache, and second processor cache

(Fig.2, 4). Moreover, Arimilli also teaches to circuitry used to recognize mapped data to cache units (Col.4: 32-40).

As per claim 7:

The system of Arimilli is constructed to detect soft errors (Col.3: 7-10). Scrubbing is a generic term for the detection and correction of soft errors in memory systems, and as such, the system of Arimilli is disposed to access each location of the main memory for error detection purposes related to soft error recognition and correction, i.e. scrubbing (Col.7: 19-35).

As per claim 8:

Arimilli teaches to a mapping system that allows for memory location detection for determining data sent to the cache circuitry, and requests reads from the communication channel between the memory and the cache circuitry (Fig.1; Col.4: 32-57; Col.7: 20-41).

As per claim 9:

The communication channel of Chaudhry is a coherent network (Fig.1B).

As per claim 10:

Chaudhry teaches to a memory system that includes a main memory controller, processor cache, a communication channel between the memory channel and the cache, and error detection and correction mechanisms within the memory controller (Fig.1B). The error detection and correction mechanism alters data and stores a corrected copy of the data in the main memory (Fig.2, 4). However, there is not an explicit teaching to the reading of a valid copy of the data checked out to the processor cache. Arimilli teaches to

reading of a valid copy of the data checked out to the processor cache and the correction of the cached data (Col.2: 10-17; Col.4: 32-52). Therefore, it would have been obvious for one of ordinary skill in the art at the time of the invention to make use of the reading of a valid copy of the data checked out to the processor cache and the correction of the cached data of Arimilli, in conjunction with the changed and re-stored data system of Chaudhry because the addition of the circuitry of Arimilli allows for faster overall operation of the circuitry by avoiding unnecessary ECC circuit operations (Arimilli: Col.4: 65-67).

As per claim 11:

Both Chaudhry [0013] and Arimilli (Col.4: 24-26) teach to single bit correction, double bit detection systems.

As per claim 12:

Arimilli (Col.4: 24-26) teaches to double bit correction systems (Col.4: 57-58).

As per claim 13:

Chaudhry teaches to I/O cache and to storage of an altered data copy in memory (Fig.2, 4). Moreover, the combination of Chaudhry with Arimilli disclosed above can further be applied here with respect to the reading of data from the cache when a copy of valid data is put into the cache, and correction of said data for re-storing in the memory.

As per claim 14:

Chaudhry teaches to a secondary processor cache and to storage of an altered data copy in memory (Fig.2, 4). Moreover, the combination of Chaudhry with Arimilli disclosed above can further be applied here with respect to the reading of data from the

cache when a copy of valid data is put into the cache, and correction of said data for re-storing in the memory.

As per claim 15:

Chaudhry teaches to circuitry that recognizes the data in the cache pulled from the memory in the cache circuitry for the processor, I/O cache, and second processor cache (Fig.2, 4). Moreover, Arimilli also teaches to circuitry used to recognize mapped data to cache units (Col.4: 32-40).

As per claim 16:

The system of Arimilli is constructed to detect soft errors (Col.3: 7-10). Scrubbing is a generic term for the detection and correction of soft errors in memory systems, and as such, the system of Arimilli is disposed to access each location of the main memory for error detection purposes related to soft error recognition and correction, i.e. scrubbing (Col.7: 19-35).

As per claim 17:

Arimilli teaches to a mapping system that allows for memory location detection for determining data sent to the cache circuitry, and requests reads from the communication channel between the memory and the cache circuitry (Fig.1; Col.4: 32-57; Col.7: 20-41).

As per claim 18:

The communication channel of Chaudhry is a coherent network (Fig.1B).

As per claim 19:

Arimilli teaches to marking a memory location when said location is read out to a cache, scrubbing the system, detecting the memory tag corresponding to a cache, reading the data from the cache, and correcting the data (Fig.1; Col.3: 7-10; Col.4: 32-57; Col.7: 20-41). Moreover, the combination of Arimilli and Chaudhry above has been shown to write the corrected results to a memory location (Fig.2, 4).

As per claim 20:

The memory checking operation of Arimilli includes accessing the memory, locating the valid copy of the data in the cache, reading the copy, and correcting errors in the data (Col.7: 20-41). Moreover, the combination of Arimilli and Chaudhry above has been shown to write the corrected results to a memory location (Fig.2, 4). The method of Arimilli teaches to the repeating of the above steps for all the cache circuitry, and as such, for their corresponding memory locations (Col.7: 35-37).

Conclusion

3. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a.	Bauer et al.	U.S. 5,604,753
b.	Springer et al.	U.S. 6,212,631
c.	Cypher	U.S. 6,304,992

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Dooley whose telephone number is (703) 306-5538. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew Dooley
Examiner AU 2133
04/07/2004

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